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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,415	09/22/2003	Gil Vinitzky	P-1912-US1	4391

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,415	VINITZKY, GIL	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 04/18/2005.

2. Claims 2-13 are pending in this application. Claims 2 and 9 are independent claims. In Amendment, claim 1 is cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-13 are rejected under 35 U.S.C. 103(a) as being obvious over Lim et al. (U.S. 6,463,451) in view of Shridhar et al. (U.S. 6,366,937).

Re claim 2, Lim et al. disclose in Figure 6 a method to calculate four results of a Fast Fourier Transform butterfly calculation (abstract and Figure 2 wherein the butterfly operation is defined), the calculation involving real and imaginary cosinusoidal data inputs, real and imaginary sinusoidal data inputs, and real and imaginary coefficients (col. 1 lines 37-47 wherein cosine and sine are involved), the method comprising: adding a first value to a first product of a real sinusoidal data input and a real coefficient and subtracting therefrom a second product of an imaginary sinusoidal data input and an imaginary coefficient to produce a first result ($Re(X_{out})$ in col. 1 line 41); and adding first

value to second product and, subtracting therefrom first product to produce a second result ($Re(Y_{out})$ in col. 1 line 45); and adding a second value to a third product of real sinusoidal data input and imaginary coefficient and to a fourth product of imaginary sinusoidal data input and real coefficient to produce a third result ($Im(X_{out})$ in col. 1 line 3); and subtracting from second value third product and fourth product to produce a fourth result ($Im(Y_{out})$ in col. 1 line 46). Lim et al. fail to disclose the FFT is performed in 2 cycles wherein the first and second results are performed in 1st cycle and the third and fourth results are performed in 2nd cycle. However, Shridhar et al. disclose in Figure 3 and in column 3 lines 10-20 that a device is capable of performing a Fast Fourier Transfer in pipelined fashion including four floating-point multiplies and additions/subtractions per clock cycle. In addition, the computation for the 4-point FFT above as cited in column 1 lines 35-47 needs only eight floating-point multiplies and several additions/subtractions operations. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to apply and arrange the 4-point FFT to perform within 2 cycles only wherein the first cycle processes four multiplications, two additions, and two subtractions for the first and second results as adding a first value to a first product of a real sinusoidal data input and a real coefficient and subtracting therefrom a second product of an imaginary sinusoidal data input and an imaging coefficient to produce a first result; and adding first value to second product and subtracting therefrom first product to produce a second result; and; and the second cycle processes another four multiplications, two additions, and two subtractions for the third and four results as adding a second value to a third product of real sinusoidal

data input and imaginary coefficient and to a fourth product of imaginary sinusoidal data input and real coefficient to produce a third result; and subtracting from second value third product and fourth product to produce a fourth result using the pipelined instruction device in Shridhar et al.'s invention into Lim et al.'s invention because it would enable to reduce the computation time (col. 1 lines 37-40).

Re claim 3, Lim et al. further disclose in Figure 6 the first value is a real cosinsoidal data input ($Re(X_{in})$ in col. 1 line 40-45 wherein X is cosinsoidal signal) and second value is an imaginary real cosinsoidal data input ($Im(X_{in})$ in col. 1 line 40-45 wherein X is cosinsoidal signal).

Re claim 4, Lim et al. further disclose in Figure 6 in first cycle: concatenating a rounding constant to a real produce first value; and in second cycle: concatenating rounding constant to an imaginary cosinusoidal data input to produce second value (86 in Figure 6).

Re claim 5, Lim et al. fail to disclose in Figure 6 in first cycle: multiplying real sinusoidal data input and imaginary coefficient to produce third product; and multiplying imaginary sinusoidal data input and real coefficient to produce fourth product. Shirdhar et al. disclose in Figure 3 a device has multiple multipliers for multiplying multiple input data (e.g. 32, 34, 36, and 38) in pipeline fashion and the pipelined operation is known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add pipelined multiplier for producing third product and fourth product in the first cycle as seen in Shirdhar et al.'s invention into Lim et al.'s

invention because it would enable to reduce the computation time (col. 1 lines 37-40) by pipeline multiplying all the products prior.

Re claim 6, Lim et al. fail to disclose in Figure 6 in second cycle: multiplying a real sinusoidal data input of a next butterfly calculation and a real coefficient of next butterfly calculation to produce a first product for next butterfly calculation; and multiplying an imaginary sinusoidal data input of next butterfly calculation and an imaginary coefficient of next butterfly calculation to produce a second product for next butterfly calculation. However, Shirdhar et al. disclose in Figure 3 a device has multiple multipliers for multiplying multiple input data (e.g. 32, 34, 36, and 38) in pipeline fashion and the pipelined operation is known in the art. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add pipelined multiplier for producing first product and second product for the next butterfly operation in the second cycle as seen in Shirdhar et al.'s invention into Lim et al.'s invention because it would enable to reduce the computation time (col. 1 lines 37-40) by pipeline multiplying all the products prior.

Re claim 7, Lim et al. further disclose in Figure 6 writing to memory first result, second result third result and fourth result within two cycles (e.g. 64, 66, 76, and 78 in addition to rationale in rejection 2).

Re claim 8, Lim et al. further disclose in Figure 6 writing first result and third result to memory in a particular cycle (e.g. 64 and 66 respectively) and second result and fourth result to memory in a next cycle (e.g. 76 and 78 respectively).

Re claim 9, it is a DSP claim of claim 1. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 1. In addition, Lim et al. further disclose in Figure 7 a first multiplier (e.g. 46), a first and second three-input arithmetic logic unit (e.g. {52, 54, 58} and {68, 70, 72}). Lim et al. fail to disclose a second multiplier. However, Shirdhar et al. disclose in Figure 3 multiple multipliers including a second multiplier for processing faster FFT. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a second multiplier as seen in Shirdhar et al.'s invention into Lim et al.'s invention because it would enable to reduce the computation time (col. 1 lines 35-40) by producing two product at a time.

Re claim 10, it is a DSP claim of claim 3. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 11, it is a DSP claim of claim 4. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 12, it is a DSP claim of claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, it is a DSP claim of claim 8. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Response to Arguments

5. Applicant's arguments filed 04/18/2005 have been fully considered but they are not persuasive.

a. The applicant argues in page 8 for claims 2 and 9 that the cited references do not disclose all the limitations cited in the claimed invention. In addition, the citation or assertion in the Office action is different than what is claimed in 2 and 9 of the subject application.

The examiner respectfully submits that the cited references clearly and logically disclose all limitations cited in the claimed invention. The Office action is further explained to clarify the rejection as seen above. In summary, the method for generating results of a complex FFT butterfly is mathematically known in the art as conventional. The only missing part or limitation of the primary reference which is disclosing the complex FFT butterfly is to perform the complex FFT butterfly in two computer cycles wherein each computer cycle requires certain operations to be performed as multiplying, adding, and subtracting. Obviously in order to achieve this method, either the clock cycle or the instruction must be adjusted to accommodate all the multiplication, addition, and subtraction in a single cycle. The secondary reference clearly discloses a method of performing FFT butterfly in two computer cycles wherein each computer cycle is capable of performing four floating-point multiplies and additions/subtractions. Thus, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to combine the primary and secondary references to use or apply and arrange the 4-point FFT to perform within 2 cycles only because it would enable to reduce the computation time.

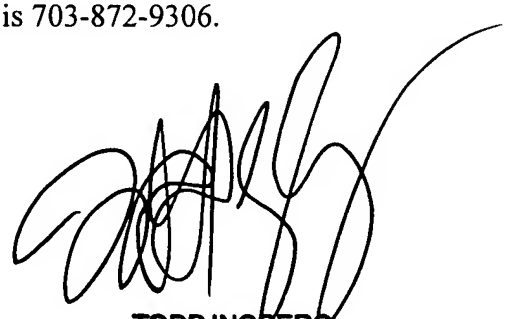
Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



TODD INGBERG
PRIMARY EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

May 19, 2005